PhD/PostDoc position on:

“Real-Time Memory Management in Latest-generation CPU+FPGA SoCs”

Brief Info:

- Laboratory: Chair of Cyber Physical Systems in Production Engineering, Technical University of Munich. (See http://www.professoren.tum.de/caccamo-marc/)  
- Supervisors: Marco Caccamo, Renato Mancuso  
- We are currently looking for motivated Ph.D. students who would like to work at TUM, Munich in collaboration with Boston University (BU)  
- Contacts: email mcaccamo@tum.de and mancuso@bu.edu

Scientific Context

Modern multi-core System-on-Chip (SoC) technologies in embedded computing systems pose new challenges for safety critical and real-time applications due to (i) increased temporal coupling between processing cores, (ii) higher degree of software integration and (iii) increased uncertainty in the hardware timing model that is used in the development and certification of embedded software for safety critical real-time systems (like avionics, autonomous automotive systems, production robots, etc.). In multi-core architectures, coupling across distinct software partitions arises because of shared hardware resources (like cache, main memory, I/O, and dedicated hardware engines), and result in loss of composability. In other words, when two software components are composed (i.e., simultaneously executed), the effect that one has on the performance of another can be significant, resulting in unexpected temporal behavior. The problem of inter-core performance interference in multicore architectures is well known and has been largely studied in literature [1, 2].

Software-level performance isolation techniques have been extensively investigated, but they come with high overheads, work at a coarse granularity, and often require complex analysis techniques to derive real-time guarantees [3]. Recently, however, hardware manufacturers have started to integrate programmable logic (FPGA) onto multi-core SoCs. The tight coupling of FPGA and traditional CPUs opens the road to a whole new set of techniques to perform smart memory resource management. In fact, one can define new hardware modules in charge of implementing high-level policies on memory traffic that are enforced at the granularity of individual memory transactions.

Research

The PhD candidate will review the existing literature on the broad topic of resource management for real-time heterogeneous SoCs, identify a specific problem (or a set of problems) he/she plan to solve, and then research, develop, and evaluate innovative resource management solutions to address the highlighted issue(s). To do this, the candidate will focus his/her attention on a specific sub-system of these complex architectures based on the preference/skills of the student and recommendations by the supervisors. While based mostly in TUM, the student will also coordinate and interact either in person or remotely with the research team at BU.

Requirements

The candidate is required to have a Master’s degree in computer science or electrical computer engineering and preferably should have a strong background in computer architecture and FPGA programming. Efficient communication skills (oral and written) in English are required. Additional useful, albeit not required expertise include real-time systems theory, operating systems, virtualization technologies, and hardware accelerators. PostDoc candidates are invited to apply as well.
Work position and application
The position is full-time and paid according to pay scale "TVOeD Bund, E 13". E14 position will be considered in case of Post Doctoral candidate with significant experience in the field of this research. The position is open to applicants worldwide.

Your complete application consists of the following documents, which should be sent as PDF files:

* CV with photo
* One-page cover letter (clearly indicating available start date as well as relevant qualifications, experience and motivation)
* University certificates and transcripts (both BSc and MSc degrees)
* Contact details of up to three referees
* Possibly an English language certificate and a list of publications

All documents should be preferably in English.

References: